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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,998	02/04/2004	Vincent Nguyen	200315049-1	4074

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EXAMINER	
LE, DIEU-MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,998	NGUYEN ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed 09/20/2006 in application 10/771,998.

2. Claims 1-27 are again presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-27 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al. (U.S. 6,092,146 hereafter referred to as Dell) in view of Huang et al. (U.S. 5,008,885 hereafter referred to as Huang).

This rejection is being applied for the same reasons set forth in the previous Office Action mailed 07/24/2006.
As per claims 1-27 see the previous office action for the detailed teaching of Dell and Huang as well as the motivation and reasons for combined.

Applicant asserts that Dell and Huang failed to teach or suggest the following:

A. **a plurality of data lines that transfer the data to and from the plurality of memory circuits;** and testing logic coupled to at least one of the plurality of data lines, wherein the testing logic utilizes data stored in the SPD memory circuit to inject a memory error **into one or more of the plurality of data lines.**

B. applying a bias voltage on at least one data line associated with the error injection procedure.

C. a plurality of means … the SPD memory circuit **to inject an error into at least one of the plurality of means for transferring data.**

Examiner respectfully transverses Applicant's argument as follows:

A. First, Examiner would like to bring Applicant attention to Dell's dynamically configurable memory for computer system [abstract, fig.1-5, col. 1, lines 5-10] comprising a connectivity among memory modules, I2C bus controller, memory controller, serial presence detects (SPDs), ect… [fig. 1-5 ,

col. 3, lines 28-50]. Dell clearly demonstrated ***the system including logic devices comprising a plurality of input and outputs via a plurality of presence detect signals from the plurality of types of memory module characteristic data into the EEPROM*** [col. 10, lines 49-53]. In addition, Huang explicitly illustrated the ***error injection*** system for testing and evaluating processes [col. 8, lines 14-34] into a ***plurality computer logic devices*** [col. 3, lines 1-17]. The combination of both Dell and Huang do teach applicant's invention (i.e., memory module with testing logic).

Second, it is ***not*** true that both Dell and Huang failed to teach "**a plurality of data lines that transfer the data to and from the plurality of memory circuits**; and testing logic coupled to at least one of the plurality of data lines, wherein the testing logic utilizes data stored in the SPD memory circuit to inject a memory error **into one or more of the plurality of data lines.**" Dell explicitly disclosed the ***logic devices comprising a plurality of input and outputs via a plurality of presence detect signals from the plurality of types of memory module characteristic data into the EEPROM*** [col. 10, lines 49-53]. Dell further illustrated the data lines that transfer the data to and from the plurality of memory circuits via its figures 3 and 4.

It is obvious to a person having ordinary skill in the art that a plurality of data and address lines are notoriously well known in the art of data computing and processing, such as memory testing.

Third, Huang's error injection is clearly illustrated in computer testing environment [col. 1, lines 1-11]. The combination of Huang's computer testing system having error injection, detection, and data recovery capabilities and Dell's dynamically configurable memory for computer system do demonstrate such applicant's invention. This is because Dell performed the ***SIMMs memory error insertion, detection, and correction means used to test memory modules*** [fig. 5, col. 4, lines 55 through col. 5, lines 19] via its plurality of data lines into the EEPROM. Therefore, it is obvious to an ordinary skill in the art to combine the Dell's error insertion and Huang's error injection to perform such memory logic testing as claimed by applicant.

Fourth, the error injection capability is well known in the memory computing environment. For example, Reynolds et al. (US 4,999,837) disclosed a programmable channel error injection into

a computer channel. In addition, Graham et al. (US 6,519,718) demonstrated a method and apparatus for implementing error injection into a plurality of data lines , busses, control logic, etc… Therefore, it is clearly to an ordinary skill in the art that the applicant's **a plurality of data lines that transfer the data to and from the plurality of memory circuits;** and testing logic coupled to at least one of the plurality of data lines, wherein the testing logic utilizes data stored in the SPD memory circuit to inject a memory error **into one or more of the plurality of data lines"** limitation is well known and readily for use in the memory testing process.

Fifth, as it clearly addressed in previous office action that it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Dell's ***SIMMs memory error insertion, detection, and correction means used to test memory modules*** as being the inject a memory error into data lines as claimed by Applicant. This is because Dell explicitly performed memory testing via error detection and correction functionality from memory insertion feature in supporting the memory/data storing, testing, evaluating, and processing. By utilizing these capabilities, the data between the data storage device or memory module and

information data communication system (i.e., host/servers/gateways/switches environment/SPD) can be directed or redirected promptly and functioned properly during error insertion or injection process in supporting the computer memory operation; second, by applying the ***error injection means used for testing and evaluating machine (i.e., processing machine, memory module, programmable devices, etc…)*** as taught by Huang in conjunction with the dynamically configurable memory for computer system as taught by Dell, the computer data memory module including row/column data lines capabilities can enhance its memory operation performance, more specifically to ensuring the best testing logic/procedure applied along with its error detected, corrected routing addresses and protocol in the storage area.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer memory operation availability and network/system performance therein with a mechanism to enhance the data processing, connectivity, data debugging, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

B. First, as indicated in previous office action that due to the similarity of claims 8-15 to claims 1-7 except for a method comprising memory module, data communication, testing logic, etc… instead of a memory module comprising memory circuit, data transferring, testing logic via applied a bias voltage, etc….; therefore, these claims are also rejected under the same rationale applied against claims 1-7. **In addition, all of the limitations have been noted in the rejection as per claims 1-7. Such as *an inter-integrated circuit (I2C) communication bus* as disclosed by Dell [fig. 3, col. 3, lines 2-3].**

Second, it is ***not*** true that both Dell and Huang failed to teach "applying a bias voltage on at least one data line associated with the error injection procedure." The combination of Huang's computer testing system having error injection, detection, and data recovery capabilities and Dell's dynamically configurable memory for computer system do demonstrate such applicant's limitation. Dell explicitly disclosed the ***SIMMs memory error insertion, detection, and correction means used to test memory modules utilizing memory row/column data input/output via its operation voltages*** [col. 5, lines 56 through col. 6, lines 15]. Dell further demonstrated the ***power-on-reset (POR) input used to support error detection and***

correction for its EEPROM [col. 3, lines 64-65] along with ***the Vcc pull up via pull-up resistor in supporting the voltage level "0" and "1" (i.e., bias voltage)*** [col. 5, lines 31-41].

Third, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to realize that the combination of Dell's ***SIMMs memory error insertion, detection, and correction means used to test memory modules utilizing memory row/column data input/output via its operation voltages*** and Huang's ***error injection means used for testing and evaluating machine*** via ***its counter machine*** (i.e., processing machine, memory module, programmable devices, etc…) ***states*** do teach applicant's counter of the number of data lines to electrically bias (voltage) limitation. This is because both Dell and Huang explicitly demonstrated memory testing via error detection/correction and injection functionality in supporting the memory/data storing, testing, evaluating, and processing. It is further obvious because Dell illustrated the data memory including row and column testing via its proper operation voltage arrangements [col. 6, lines 9-11]. By utilizing these capabilities, the computer data memory module including row/column data lines capabilities can enhance its memory

operation performance, reliability, and maximizing its throughput.

C. First, it is ***not*** true that both Dell and Huang failed to teach "a plurality of means … the SPD memory circuit **to inject an error into at least one of the plurality of means for transferring data**". This is because Dell clearly demonstrated ***the system including logic devices comprising a plurality of input and outputs via a plurality of presence detect signals from the plurality of types of memory module characteristic data into the EEPROM*** [col. 10, lines 49-53]. In addition, Huang explicitly illustrated the ***error injection*** system for testing and evaluating processes [col. 8, lines 14-34] into a ***plurality computer logic devices*** [col. 3, lines 1-17]. The combination of both Dell and Huang do teach applicant's invention (i.e., memory module with testing logic). Therefore, the combination of both Dell and Huang do teach applicant's invention (i.e., **inject an error into at least one of the plurality of means for transferring data**).

Second, The combination of Huang's computer testing system having error injection, detection, and data recovery capabilities and Dell's dynamically configurable memory for

computer system do demonstrate such applicant's limitation. Dell explicitly disclosed the ***SIMMs memory error insertion, detection, and correction means used to test memory modules utilizing memory row/column data input/output via its operation voltages*** [col. 5, lines 56 through col. 6, lines 15]. Dell further demonstrated the ***power-on-reset (POR) input used to support error detection and correction for its EEPROM*** [col. 3, lines 64-65] along with ***the Vcc pull up via pull-up resistor in supporting the voltage level "0" and "1" (i.e., bias voltage)*** [col. 5, lines 31-41]. Therefore, the combination of both Dell and Huang do teach applicant's invention (i.e., **inject an error into at least one of the plurality of means for transferring data**).

Applicant's arguments filed 09/20/2006 have been fully considered but they are not persuasive.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R.

§ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644.
The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

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